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(54) Image processing apparatus.

(57) A priority circuit determines a priority order of images for each dot, the images being supplied from a variety of image generators. In accordance with the priority order, the images are displayed on a screen.

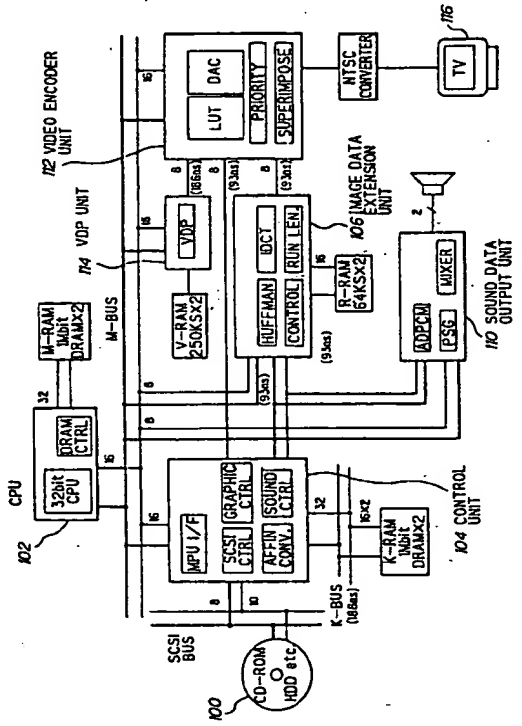

FIG. 2

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BACKGROUND OF THE INVENTION

The present invention relates to an image processing apparatus, and more particularly to an image processor used in a game computer system.

In a conventional game computer, an image processing operation is carried out mainly by an external memory, a CPU (central processing unit), a VRAM (video RAM), a VDC (video display controller), a VDE (video encoder) and a CRT. In this type of computer, image data are transmitted from the external memory to the VRAM, and are read from the VRAM by the CPU.

In one type of conventional game computer, each image is composed of background and sprite pictures, the background picture being formed in accordance with a character pattern defined by a raster of the CRT and character pitch. In the memory (RAM), the background and sprite images are managed by using background and sprite attribute tables BAT and SATB and character and sprite generators CG and SG, respectively.

The BAT is composed of a "CG color" of 4 bits and a "character code" of 12 bits, to specify positions and colors of the characters to be displayed. The CG is incorporated in the RAM for storing four actual character patterns corresponding to CG codes in the BAT. Each character pattern is defined by 8 × 8 dots and 16 colors. The SATB is composed of a "sprite color" and a "pattern code," the pattern code specifying a corresponding SG. The SG defines an actual sprite pattern.

In such a game computer, an address of the raster position to be displayed is generated first, and then the character code and CG color are given in accordance with the address. An address of the CG is produced in accordance with the character code. The pattern data stored in the CG are read out in accordance with the CG address, and are transmitted with the CG color code to the following stage. The sprite pattern codes and SG color codes are read from the SATB in the order of the address. An address of the SG is produced in accordance with the sprite pattern code as well as the background image. When coordinate data specifying a display position or whole data of the SATB are changed, an image to be displayed on the CRT varies.

When the sprite and background image data are supplied to a priority circuit, these data are superimposed on each other in accordance with an instruction held in a priority register.

When display data including the CG pattern data, CG color code, SG pattern data and SG color code are supplied from the VDC to the VDE, the display data are converted to the RGB signal by a D/A converter in accordance with the contents of a color pallet RAM. The color pallet RAM stores RGB digital data written by the CPU.

Fig. 1 shows the structure of the color pallet RAM, which includes color pallets of "256 addresses × 9 bits," and is divided into 16 blocks of "16 addresses × 9 bits." The RGB data are stored in the 9 bit area. That is, each color of the RGB has data of 3 bits, and one dot is defined by one address. Each block has 16 colors selected from 256 colors. In the color pallet RAM, one of the color blocks is specified by the color code to selected 16 colors to be used from 256 colors, and a color to be used is specified from the 16 colors by the pattern data.

In the conventional game computer system, the background and sprite pictures are produced with the same dot cycle in the same unit so that they have the same format. Such background and sprite image data are transmitted to the priority circuit in synchronization with dot clocks, which are used for displaying the images on the CRT. If a variety of image data generators are used, however, the transmission timing must be changed depending on the image data, because many kinds of image data which need different processing times are supplied to the priority circuit.

Recently, a variety of kinds of image data have been required to be displayed in a multi media computer system. According to the conventional system, however, only colored image data are treated, that is, transparent image data are not treated.

In the conventional system, in order to realize fade-in and fade-out processing, generally, the next picture is faded in the CRT after the previous picture has been faded out from the CRT. Further, in order to realize cross fade processing, in which the previous picture is faded out from the CRT by fading the next picture in the CRT, the two pictures are controlled in brightness gradually (in analog fashion) by using an attenuator or the like.

The conventional computer system performs cellophane processing, in which upper and lower pictures (front and back cellophane) are synthesized by an arithmetic operation in accordance with predetermined priority information.

Cellophane arithmetic results Y, U and V are given by the following equations, where Ya, Ua and Va indicate data of a picture to be synthesized on Yb, Ub and Vb data, the Yb, Ub and Vb indicate data of a picture to be synthesized with the Ya, Ua and Va and my, mu, mv, nuy, nv and nu indicate cellophane coefficients, respectively:

$$Y = my \times Ya + ny \times Yb$$

$$U = mu \times (Ua - 80h) + nu \times (Ub - 80h) + 80h$$
$$V = mv \times (Va - 80h) + nv \times (Vb - 80h) + 80h$$

In the above equations, "80h" of the U and V are treated as "0". Each of the Y, U and V becomes "FFh" and "00h" if it is overflown and underflown, respectively.

According to the conventional computer system, however, the cellophane function is not performed for each sprite character.

SUMMARY OF THE INVENTION

It is an object of the present inveiition to provide a high performance image processing apparatus, in which a priority circuit may effectively process a variety of image data supplied from different kinds of image generators.

It is another object of the present invention to provide a high performance image processing apparatus, which may deal with a variety of color data including transparent image data.

It is still another object of the present invention to provide an image processing apparatus, by which a high performance cellophane function may be realized.

According to a first feature of the invention, a priority circuit determines a display order of images for each dot, the images being supplied from a variety of image generators. In accordance with the priority order, the images are displayed on a screen.

According to a second feature of the invention, an image processing apparatus includes a register for specifying a key area to be displayed as being transparent. A plurality of images are synthesized in accordance with the data held in the register.

According to a third feature of the invention, a video display processor (VDP) processes color data of an image to be displayed, and a video encoder unit synthesizes a plurality of images in a predetermined order of a display priority by a cellophane function. The cellophane function is controlled to be turned on and off for each unit of a predetermined data block (color pallet bank).

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a diagram showing the configuration of a color pallet RAM.

Fig. 2 is a block diagram showing a computer system according to the invention.

Fig. 3 is a block diagram showing a video encoder unit in the computer system shown in Fig. 2.

Fig. 4 is a diagram showing the configuration of a color pallet RAM, accordance to the invention.

Fig. 5 is an explanatory diagram showing a process for producing a color pallet address, in accordance with the invention.

Fig. 6 is a table showing color pallet data in accordance with the invention.

Fig. 7 is an explanatory diagram showing a priority process in a 256 dots mode, according to the invention.

Fig. 8 is an explanatory diagram showing a chromakey process, according to the invention.

Fig. 9A is a block diagram showing a cellophane function according to the invention.

Fig. 9B is a table showing data chroinakey processes of the VDP unit, control unit and image data extension unit, according to the invention.

Fig. 10 is a flow chart showing operation of the cellophane function, according to the invention.

Fig. 11 is an explanatory diagram showing the cellophane function, according to the invention.

Fig. 12 is an explanatory diagram showing a front cellophane function, according to the invention.

Fig. 13 is an explanatory diagram showing a back cellophane function, according to the invention.

Figs. 14 to 16 and 18 to 25 are diagrams showing the configurations of an address register, status register, control register, color pallet address register, color pallet data write register, color pallet address offset register 1, color pallet address offset register 2, color pallet address offset register 3, color pallet address offset register 4 and two priority registers, respectively, according to the invention.

Fig. 17 is a table showing information on the interlace and non-interlace modes, according to the invention.

Figs. 26 to 28 are diagrams showing the configurations of chromakey-Y, chromakey-U and chromakey-V registers, respectively, according to the invention.

Fig. 29 is a diagram showing the configuration of a fixed color register, according to the invention.

Fig. 30 is a diagram showing the configuration of a cellophane image setting register, according to the invention.

Figs. 31 to 37 are diagrams showing detail of the cellophane image setting register, shown in Fig. 30.

Fig. 38 is a diagram showing the configuration of a special cellophane setting register, according to the invention.

Fig. 39 is a diagram showing the configuration of a cellophane coefficient register, according to the invention.

Fig. 40 is a diagram illustrating an image displayed in the non-interlace mode, according to the invention.

Fig. 41 is a diagram illustrating an image displayed in an interlace mode, according to the invention.

Fig. 42 is a diagram illustrating an image displayed in the interlace + 1/2 dot shift mode, according to the invention.

DETAILED DESCRIPTION OF THE INVENTION

Hereinafter, an image processing apparatus of a preferred embodiment according to the present invention will be explained in conjunction with appended drawings.

Fig. 2 shows a computer system of the preferred embodiment. The system includes a game-software recording medium 100 such as a CD-ROM, a CPU 102 of 32-bit type, a control unit 104 for mainly controlling transmission of image and sound data and interfacing most devices to each other, an image data extension unit 106, an image data output unit 108, a sound data output unit 110, a video encoder unit 112, a VDP unit 114 and a TV display 116. CPU 102, control unit 104, image data extension unit 106 and VDP unit 114 are provided with their own memories K-RAM, M-RAM, R-RAM and V-RAM, respectively.

CPU 102 directly controls a DRAM via a memory support, and performs communication through an I/O port to peripheral devices, that is, an I/O control function. CPU 102 includes a timer, a parallel I/O port and a interruption control system. VDP unit 114 reads display data which have been stored in the VRAM by CPU 102. The display data are transmitted to video encoder unit 112 whereby the data are displayed on the TV display 116.

Control unit 104 includes an SCSI controller to which image and sound data are supplied from CD-ROM 100 through an SCSI interface. Data supplied to the SCSI controller is buffered in the K-RAM. Control unit 104 also includes a DRAM controller for reading data which have been buffered in the K-RAM, at a predetermined timing. In control unit 104, priority judgement is carried out for each dot of natural background image data, and an output signal is transmitted to video encoder unit 112.

Control unit 104 transmits moving image data (full color, pallet), which has been reduced, to image data extension unit 106 whereby the scale-down data are extended. The extended data are transmitted from image data extension unit 106 to video encoder unit 112.

Video encoder unit 112 superimposes VDP image data, natural background image data and moving image data (full color, pallet) transmitted from VDP unit 114, control unit 104 and image data extension unit 108, respectively. Video encoder unit 112 performs color pallet reproducing, special effect processing, D/A converting and the like. Output data of video encoder unit 112 are encoded into an NTSC signal by an external circuit.

ADPCM sound data which have been recorded in CD-ROM 100 are buffered in the K-RAM and then transmitted to sound data output unit 110 by control unit 104. The sound data are reproduced by sound data output unit 110.

Fig. 3 shows the video encoder unit, which is composed of an IC including a synchronizing signal generating circuit, a color pallet RAM, a priority arithmetic circuit, a cellophane arithmetic circuit (for synthesizing upper and lower pictures), a D/A converter for an image signal, an 8/16 bit data bus (M-bus) interface, a VDP interface, a control unit interface and an image data extension unit interface.

The 8/16 bit data bus interface is an I/F switching circuit which selects one from 8 and 16 bit data buses to be used for data processing at the video encoder unit side. The selection is carried out in accordance with data width of the data bus of the processing system including the CPU.

The VDP interface receives data transmitted from two of upper and lower VDPs. Normally, the VDP interface receives data from the upper VDP. The VDP interface receives data from the lower VDP only when the upper VDP supplies chromakey data.

The color pallet RAM transforms a video input signal into a YUV digital signal.

The video encoder unit has registers (16 bits × 24 lines), which are accessed by the CPU to set an operation mode therein, and to specify read and write modes for the color pallet.

The color pallet RAM transforms color pallet data into YUV data to be actually displayed, as mentioned before. As shown in Fig. 4, the color pallet RAM includes a color information table divided into 512 address regions each having one color and 16 bit data regions. Each color data are composed of 8 bits "Y", 4 bits "U" and 4 bits "V", so that 65536 colors may be available. The "Y" data indicate brightness in a range 00 (black) to FF (white), the "U" data indicate color difference for a blue-to-yellow family in a range 0 to 15, and the "V" data indicate color difference for a red-to-green family in a range 0 to 15. Each of the U and Y data are set at a value 8 when no-color is represented. After the reset process, YY = 00h, U = 0h and V = h are automatically set at the "0" of the color pallet address. For that reason, color data need to be set at the address 0 again after

the reset process.

How to set the YUV data at the color pallet RAM is now explained. The contents of the color pallet RAM are formed by the CPU, and are read in accordance with color pallet information from the VDP, control unit and image data extension unit. The read data are transformed into the Y, U and V data. The CPU can read the contents of the color pallet RAM.

The data are written in the color pallet RAM continuously in accordance with the following steps:

1st step : Setting a register number "01h" of a color pallet address register (CPA) in an address register (AR).

2nd step : Writing a start address in the color pallet address register (CPA).

3rd step : Writing a register number of a color pallet data write register (CPW) in the address register (AR).

4th step : Writing data in the color pallet data write register to increment the CPA.

5th step : Writing data in the color pallet data write register again to increment the CPA.

In the 8 bit bus mode, data are written in the data write register in the order of lower to upper bytes. After the upper bytes data are written in the data write register, the data are written in an internal register, and the CPA is incremented.

Next, how to display the color pallet data will be explained. The color pallet data stored in the VDP, control unit and image data extension unit are transformed to the YUV data in accordance with the contents of the color pallet RAM to form an actual image. All screens using the color pallet data are treated by the common color pallet RAM because only one color pallet RAM is provided. If a color pallet address offset register is used, color pallet start addresses may be specified for each picture separately.

In a priority process block, a picture to be displayed is specified for each dot. If the specified picture is a color pallet data picture, a color pallet address offset value of the picture is read from the register. After that, double the offset value is added to the color pallet data to provide a color pallet address. In accordance with the color pallet address, the color data Y, U and V are generated for each dot, and are transmitted to the following stage.

Even though the same color pallet data are used for the different pictures, different colors may be generated for the pictures.

The VDP has only one color pallet offset register, so that if plural VDPs are used, the plural VDPs have to use the single register in common. If the color pallet address is over 511, the tenth bit is omitted, that is, the ninth bit is connected to 0 address, as shown in Fig. 5. When the CPU accesses the color pallet RAM directly, the color pallet address offset is not effective.

Fig. 16 shows the contents of color pallet data transmitted from each of the LSIs. In a calculation of a color pallet address, a pallet bank number is treated as the first bits of a pallet number, that is, the pallet and pallet bank numbers are not distinguished from each other. Therefore, all 8 bits data in each mode are treated as the color pallet data.

In this preferred embodiment, the VDP unit treats two kinds images of the sprite (SP) and background (BG), the control unit treats four images BMG0, BMG1, BMG2 and BMG3, and the image data extension unit treats an IDCT/RL image, respectively. The video encoder unit may be connected with the upper and lower VDPs. If both the upper and lower VDPs are connected to the video encoder, one of the VDPs is selected to be connected at an input interface portion. The upper VDP is generally selected and the lower VDP is selected only when the upper VDP supplies chromakey data.

The priority order of the SP and BG images of the VDP and the pictures BMG0 to BMG3 can not be changed only by the priority register of the video encoder unit. Therefore, if the priority order is changed, all the units must be changed.

The priority order is decided for each dot by the video encoder unit in accordance with image information, the value of the priority register, whether the color is chromakey, and the like, the image information being transmitted from the VDP, control unit and image data extension unit.

Fig. 7 shows priority processing in the 256 dots mode. In this embodiment, the priority process is carried out using a clock of four times the dot clock, in addition to special processes such as the chromakey process and cellophane process. In the cellophane process, upper and lower pictures (front and back cellophane) are synthesized when the video encoder synthesizes some images in accordance with the priority.

In the 320 dot mode, each of the control unit and image data extension unit has 256 dots and the VDP has 320 dots. Therefore, an image to be displayed is specified in the period of 21MHz and the image (device) is displayed immediately.

In the chromakey function (transparency process), some portions of an image are treated as transparency portions, on which low priority pictures are displayed. Actually, a color to be judged as a transparency (key color) is defined in advance. The key color differs depending on the type of data, color pallet data, IDCT-YUV data or YUV data of the control unit. To use no chromakey function is equivalent to use no key color when a

picture to be displayed is drafted.

Fig. 8 shows operation of the chromakey function. If a color pallet data 0 (pallet number 0 in VDP) is used as the key color, the color pallet data 0 is treated as a transparency color at the run-length region in the control unit and image data extension unit in any mode. In the VDP, regions of pallet number 0 are treated as transparency at any color pallet bank.

Figs. 9A and 9B show the above mentioned chromakey operation. In some cases, the control unit performs chromakey judgement and supplies an invalid signal to the color pallet data picture. If Y-data of YUV data are set "00h" on a dot in the control unit (in the 16M color mode and 64K color mode), the dot is displayed with transparency color independently of values for U and V data. A value of "01h" or the like is added to the Y-data at regions not to be displayed with transparency in order that the Y-data does not have a value "00h". If an intermediate color located between a chromakey highest register value and a chromakey lowest register value is selected as the key color for the IDCT-YUV data screen and all of the YUV values to be displayed are located between the two register values, the selected color is judged as the key color, and as a result, the region is displayed with transparency color.

Specifically, in the case where the highest and lowest values of the chromakey Y register are Yu and Yl, the highest and lowest values of the chromakey U register are Uu and Ul, the highest and lowest values of the chromakey V register are Vu and Vl and Y, U and V values to be displayed are Ys, Us and Vs, a color to be displayed is the key color if all of the following equations are true.

$$Yu >= Ys >= Yl$$
$$Uu >= Us >= Ul$$
$$Vu >= Vs >= Vl$$

When invalid signals are transmitted from the control unit and image data extension unit to the video encoder, the dots corresponding to the invalid signals are treated the same as the case of key color, that is, the dots are displayed with transparency color. The chromakey portion on the lowest priority region is displayed with a color which will be used for the following portion in accordance with the priority process. Therefore, the following picture is displayed instead of the present one if all pictures including YUV data pictures are transparency. In the same manner, the chromakey region on the lowest priority picture is cellophane processed.

Fig. 10 shows the cellophane function, which is for superimposing upper and lower pictures in accordance with the priority information stored in the video encoder. In the operation of cellophane function, when the cellophane function is set at 0 picture in the control unit, a lower priority picture is mixed with the 0 picture, so that the 0 picture is displayed with half-transparency color. It is possible to realize fade-in processing, fade-out processing and smoothly changing of pictures by varying the mix ratio of the cellophane function.

The cellophane coefficient may be divided into 9, 0/8 to 8/8 so that the cellophane coefficient may be varied by changing the numerator. The cellophane coefficient is established by certain software.

A cellophane coefficient register is provided with 3 regions each having 6 parameters. When the cellophane function is set to a certain picture, the cellophane coefficient number (1 to 3) is written in a specified portion of the register. If "0" is set at the specified portion, the picture is separated from the cellophane function. Values 9 to F for the cellophane coefficient register are not supported.

The cellophane arithmetic is not carried out to a chromakey portion of a picture to be overlapped with another picture, so that the general chromakey process is carried out to the overlapped picture. According to the cellophane function, it is possible to realize functions of multi-cellophane, front cellophane, back cellophane and sprite special. In the multi-cellophane function, the cellophane process is carried out again on a picture which has been processed by the cellophane function. In the front cellophane function, the whole screen is changed in color and in brightness by the cellophane function using a pre-selected color. In the back cellophane function, the cellophane process can be carried out on a picture having the lowest priority. In the sprite special process, the cellophane function can be used on the sprite picture for each pallet bank.

According to a sprite special function, the cellophane function on the sprite image may be controlled ON and OFF in accordance with a pallet bank number of the sprite image. That is, the cellophane arithmetic operation may be controlled for each pallet bank number.

The cellophane process is carried out for each dot, as shown in Fig. 11. The VDP unit, control unit and image data extension unit supply first to third pictures I to III, the correspondence being arranged for each dot in accordance with picture priorities supplied from the units.

For example, if the priority is set on a dot in the order of "VDP > control unit > image data extension unit", the third picture III is used for the VDP unit, the second picture II is used for the control unit and the first picture I is used for the image data extension unit, respectively. In this case, when the cellophane instruction is set on the second picture II (for example, the BMG1 picture of the control unit), the cellophane process is carried out on the first and second pictures I and II in accordance with the cellophane coefficient, which corresponds to the value set in the coefficient register of the second picture II. Further, if the cellophane instruction is set

In these steps, the content of the address register is maintained at the current value until the address register is rewritten. Therefore, the first step may be omitted when the same register is again accessed.

When the address register is read, the register is changed to the status register. The status register holds information such as the raster count value and interlace state.

The data bus to be used is selected between 8 and 16 bit types by an EX8/-16 terminal. While the 8 bit type is used, lower and upper bytes of the register are accessed by setting an A0 terminal at "0" and "1", respectively. On the other hand, while the 16 bit type is used, the level at the A0 terminal is ignored, because 16 bits data can be accessed directly.

Figs. 18 to 25 show the configurations of a color pallet address register, color pallet data write register, color pallet address offset register 1, color pallet address offset register 2, color pallet address offset register 3, color pallet address offset register 4, priority register 1, and priority register 2, respectively.

The color pallet address register (CPA : R01) holds a color pallet address to be used when the color pallet RAM is accessed by the CPU, as shown in Fig. 18. The color pallet data write register and color pallet data read register are accessed in accordance with the color pallet address held in the color pallet address register. The color pallet address register is automatically incremented each time after the color pallet data write and read registers are accessed.

The color pallet data write register (CPW : 02) holds YUV data to be written at the address CPA in the color pallet RAM by the CPU, as shown in Fig. 19. Each of the Y, U, and V data are indicated by positive whole numbers. Each of the U and V data are treated as 8 bits data by adding "0000" at the end thereof, because the D/A converter treats 8 bits data only. The writing process may carried out continuously by the automatic increment function of the color pallet address register.

When the 8 bit data bus is used, the writing process is carried out in the order of the last half bytes to the first half bytes, because the data are written in the register after the writing process for the first half data is carried out. The increment process of the CPA is also carried out after the first half data are written in the register.

The color pallet data read register (CPR : R03) holds YUV data to be read from the color pallet RAM by the CPU. The reading process may carried out continuously by the automatic increment function of the color pallet address register.

When the 8 bit data bus is used, the reading process is carried out in the order of the last half bytes to the first half bytes, because the increment process is carried out after the first half data are read out.

The color pallet address offset register 1, shown in Fig. 20, is used for specifying which color pallet is used first for each unit of the VDP pictures. Actually, a double value of that held in the register is used as the offset value for the color pallet address. The address offset value is available from the following horizontal display period.

$$\text{SP color pallet address} = \text{SP color pallet data} + (\text{SP color pallet offset}) \times 2$$
$$\text{BG color pallet address} = \text{BG color pallet data} + (\text{SP color pallet offset}) \times 2$$

The color pallet address offset register 2, shown in Fig. 21, is used for specifying which color pallet is used first for each unit of the image pictures supplied from the control unit. In this register, offset values are set for BM0 and BM1, respectively.

Actually, a double value of that held in the register is used as the offset value for the color pallet address. The address offset value is effective from the following horizontal display period.

$$\text{BMG0 color pallet address} = \text{BMG0 color pallet data} + (\text{BMG0 color pallet offset}) \times 2$$
$$\text{BMG1 color pallet address} = \text{BMG1 color pallet data} + (\text{BMG1 color pallet offset}) \times 2$$

The color pallet address offset register 3, shown in Fig. 22, is also used for specifying which color pallet is used first for each of the image pictures supplied from the control unit. In this register, offset values are set for BM2 and BM3, respectively.

Actually, double values of that held in the register are used as the offset values for the color pallet address. The address offset values are effective from the following horizontal display period.

$$\text{BMG2 color pallet address} = \text{BMG2 color pallet data} + (\text{BMG2 color pallet offset}) \times 2$$
$$\text{BMG3 color pallet address} = \text{BMG3 color pallet data} + (\text{BMG3 color pallet offset}) \times 2$$

The color pallet address offset register 4, shown in Fig. 23, is used for specifying which color pallet is used first for each run-length picture supplied from the image data extension unit.

Actually, a double value of that held in the register is used as the offset value for the color pallet address. The address offset value is effective from the following horizontal display period.

$$\text{The color pallet address} = \text{run - length color pallet data} + (\text{run - length color pallet offset}) \times 2$$

The priority registers 1 and 2, shown in Figs. 24 and 25, hold data of 3 bits for specifying priority orders of image pictures to be displayed. In these registers, a larger figure has higher priority and a lower figure has lower priority. The same figure is not allowed to be set in the different registers.

Figs. 26 to 28 show chromakey-Y, chromakey-U and chromakey-V registers for the IDCT screen, respectively. The chromakey-Y (brightness) register, shown in Fig. 26, stores data for specifying the upper and lower limits of a Y component in the chromakey function. In this register, "00H" and "FFH" represent black and white, respectively, these data being effective from the next horizontal display period.

The chromakey-U (color difference) register, shown in Fig. 27, stores data for specifying the upper and lower limits of a U component in the chromakey function. In this register, set data are effective from the next horizontal display period.

The chromakey-V (color difference) register, shown in Fig. 28, stores data for specifying the upper and lower limits of a U component in the chromakey function. In this register, set data are effective from the next horizontal display period.

Fig. 29 shows a fixed color register (CCR : R0D), which is used for the front and back cellophane processing. The register stores Y data of 8 bits, U data of 4 bits and V data of 4 bits to specify a color, the data being set by the positive whole numbers. In this register, set data are effective from the next horizontal display period.

Fig. 30 shows a cellophane setting register (BLE : R0E), in which set data are effective from the next horizontaldisplay period.

Fig. 31 to 37 show detail of the cellophane setting register, shown in Fig. 30.

Fig. 38 shows an SP cellophane setting register (SPBL : R0F). When the register specifies a color pallet bank (block) to be cellophane OFF, a sprite picture using the color pallet bank is not processed by the cellophane function. This register is effective only when a cellophane ON is set for the sprite picture in the cellophane setting register.

Fig. 39 shows a cellophane coefficient register, in which three pairs of data (1A, 1B), (2A, 2B) and (3A, 3B) are used. Each of Y, U and V data are divided into 9, "0/8" to "8/8," so that the coefficient may be varied by changing the numerator.

As mentioned before, according to the invention, the priority processing is performed for each unit of predetermined dots, and therefore, plural pictures which are composed of different numbers of dots may be superimposed on each other. Further, this system may use the cellophane and chromakey processing together with the priority function, and as a result, high performance image processing may be realized.

A cellophane coefficient register is provided with 3 regions each having 6 parameters. When the cellophane function is set to a certain picture, the cellophane coefficient number (1 to 3) is written in a specified portion of the register. If "0" is set at the specified portion, the picture is separated from the cellophane function. Values 9 to F for the cellophane coefficient register are not supported.

Fig. 40 shows image displayed in the non-interlace mode, and Figs. 41 and 42 show images displayed in a general interlace mode and in the interlace mode with a 1/2 dot shift function, which will be explained later.

The video encoder may select an interlace mode, which is used for TV in general, and a non-interlace mode. In the interlace mode, scanning lines are fixed in number at 263 or 262, an O/E bit at a status register is "1" in an odd field period in first 1/60 seconds so that an image is displayed as in the non-interlace mode. In the next 1/60 second, that is in an even field period, an O/E bit becomes "0" to display an image located 1/2 line above the previous image. As a result, the distance between the first (odd) field and second (even) fields becomes narrow, and the image is displayed smoothly. In the same manner, these processes are repeated alternatively. If the odd and even fields have the same pictures, the image is displayed as if it seems being vibrated up and down with short interval. Image data are displayed field by field whereby the desired image is obtained.

In the interlace mode, it is possible to display a more higher quality image by using the 1/2 dot shift function therewith. According to the 1/2 dot shift function, picture elements are shifted 1/2 dot in a horizontal direction at one line interval. In this function, a mask is used for smoothing notched edge lines of the image, so that the displayed image is composed of 255.5 dots.

Claims

1. An image processing apparatus, which includes a plurality of image generators, comprising:
   a priority circuit for determining a display order of images for each dot, the images being supplied from the image generators; and
   means for displaying the images in accordance with the priority order.

2. An image processing apparatus which deals with a plurality of images simultaneously, comprising:
   a register for specifying a key area to be displayed as being transparent; and

an image data output unit which superimposes a plurality of images in accordance with data held in the register.

3. An image processing apparatus, according to claim 2, further comprising:
a register for specifying a degree of transparency, according to which the image data output unit superimposes the images.

4. An image processing apparatus, comprising:
a video display processor (VDP) for processing color data of an image to be displayed;
a video encoder unit, which synthesizes a plurality of images in a predetermined order of a display priority by a cellophane function; and
means for controlling the cellophane function to be turned on and off for each unit of a predetermined data block (color pallet bank).

FIG. 1 PRIOR ART

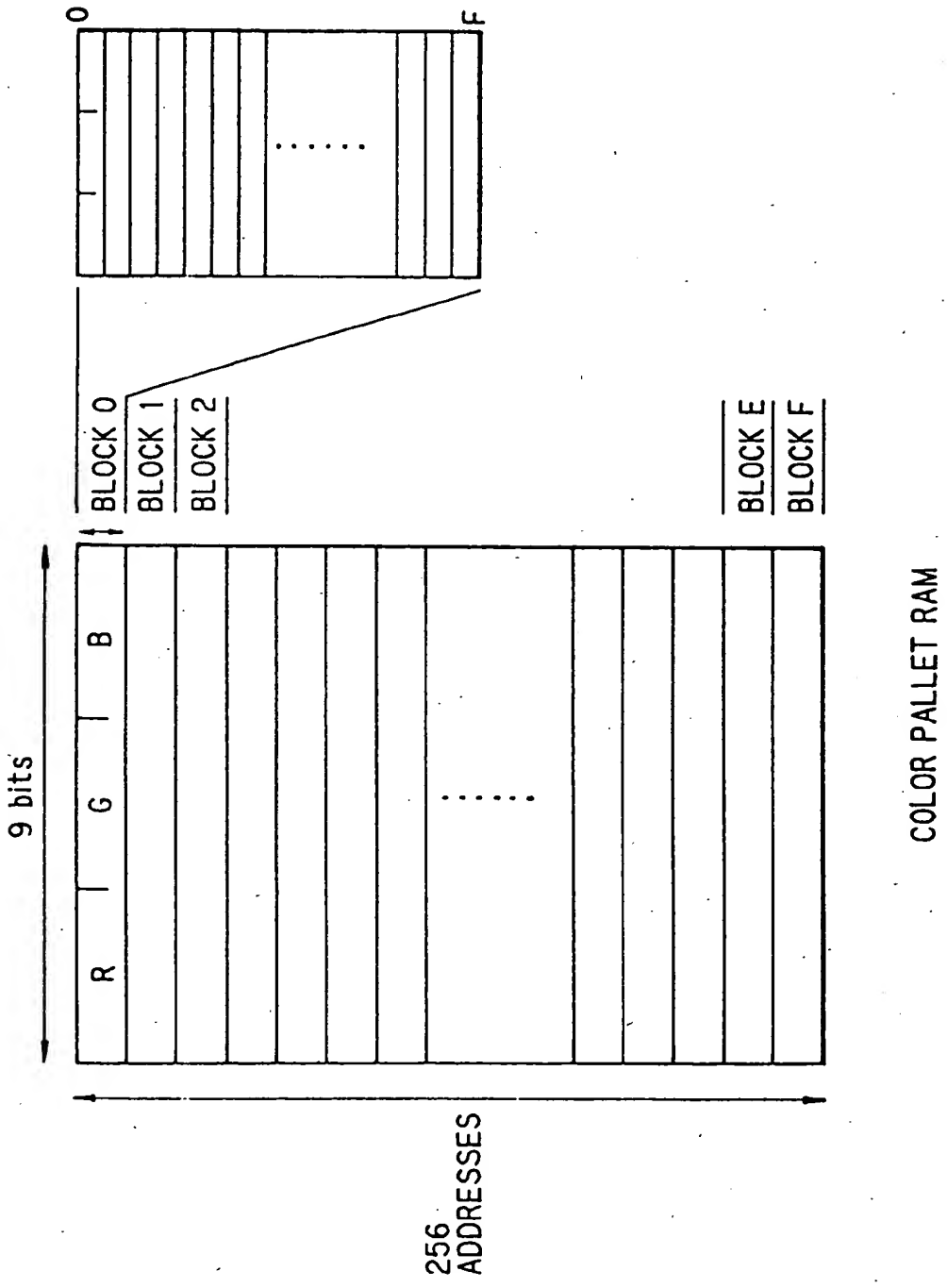

FIG. 2

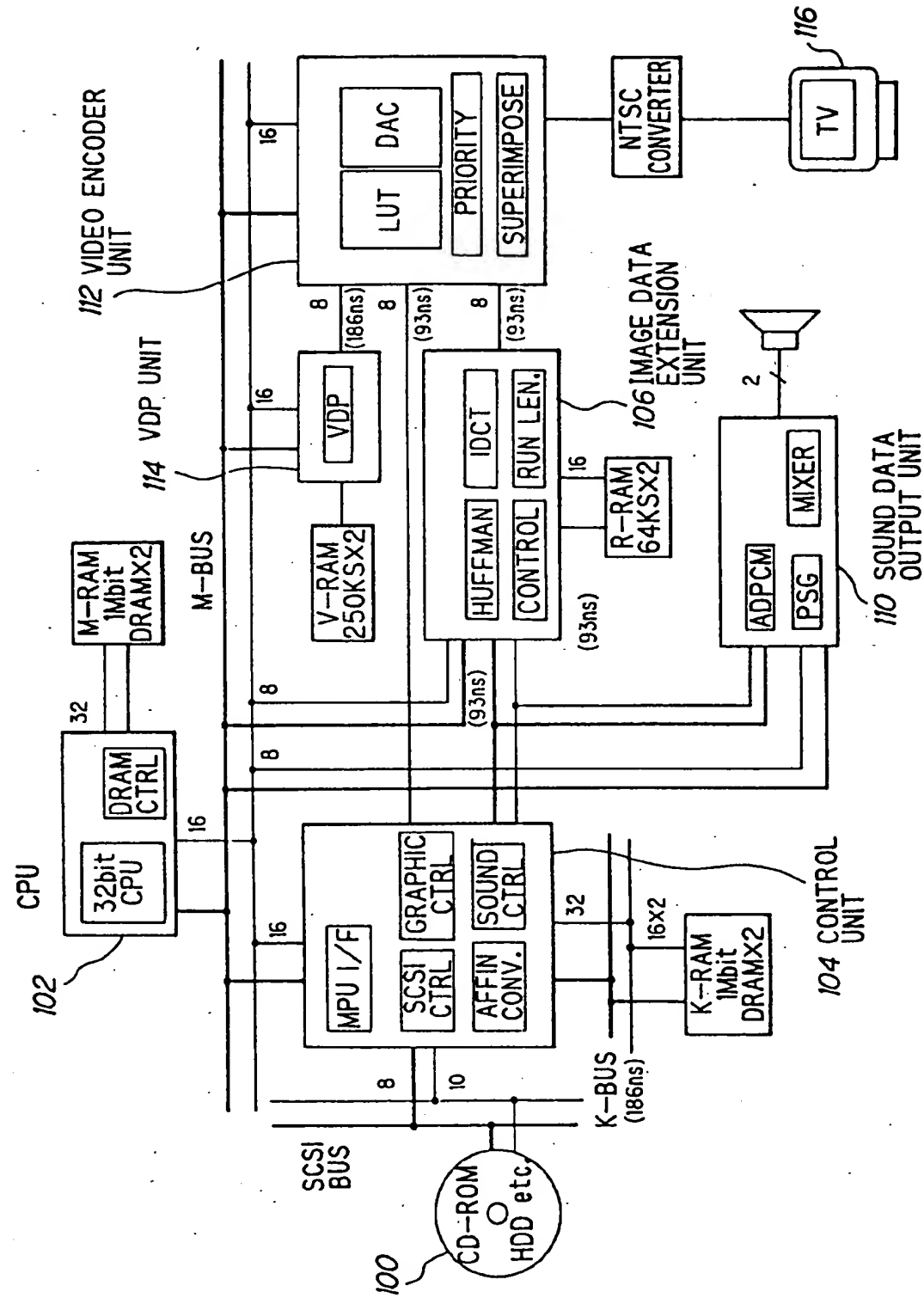
112 VIDEO ENCODER UNIT
LUT
DAC
PRIORITY
SUPERIMPOSE
NTSC CONVERTER
TV
116
114 VDP UNIT
VDP
V-RAM 250KSX2
106 IMAGE DATA EXTENSION UNIT
IDCT
RUN LEN.
HUFFMAN
CONTROL
R-RAM 64KSX2
2
MIXER
ADPCM
PSG
110 SOUND DATA OUTPUT UNIT
M-RAM 1Mbit DRAMX2
M-BUS
CPU
32bit CPU
DRAM CTRL
102
MPU I/F
GRAPHIC CTRL
SOUND CTRL
SCSI CTRL
AFFIN CONV.
104 CONTROL UNIT
16x2
K-RAM 1Mbit DRAMX2
K-BUS (186ns)
SCSI BUS
CD-ROM HDD etc.
100
8
16
32
10
(186ns)
(93ns)

FIG. 4

COLOR PALLET RAM

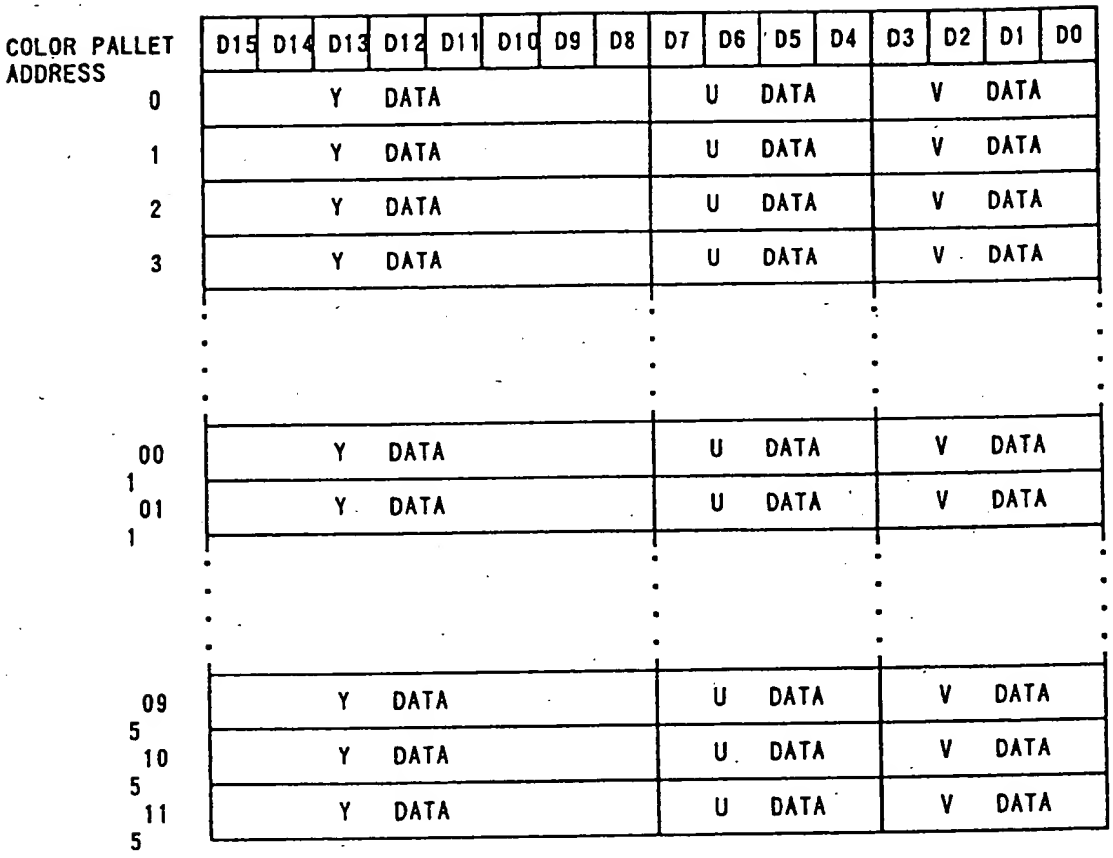

FIG. 5

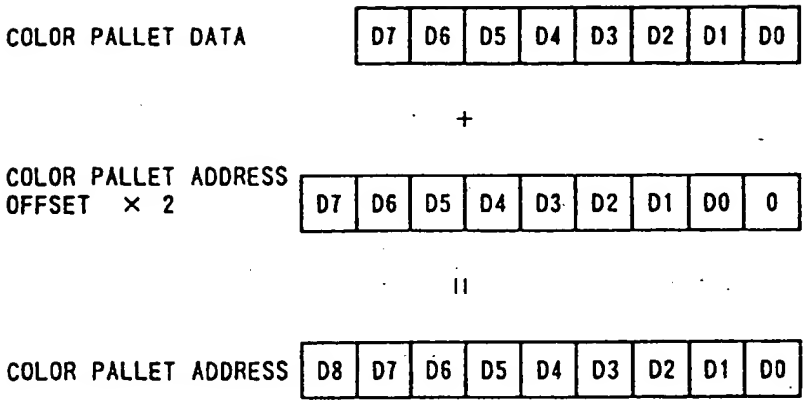

FIG. 6

PICTURE		D7	D6	D5	D4	D3	D2	D1	D0
VDP	SPRITE	PALLET BANK No.				PALLET No.			
	BG	PALLET BANK No.				PALLET No.			
CONTROL UNIT	4 COLOR MODE	0	0	PALLET BANK No.				PALLET No.	
	16 COLOR MODE	PALLET BANK No.				PALLET BANK No.			
	256 COLOR MODE	PALLET No.							
IMAGE DATA EXTENSION UNIT (RL SCREEN)	16 COLOR MODE	0	0	0	0	PALLET No.			
	32 COLOR MODE	0	0	0	PALLET No.				
	64 COLOR MODE	0	0	PALLET No.					
	128 COLOR MODE	0	PALLET No.						

FIG. 7

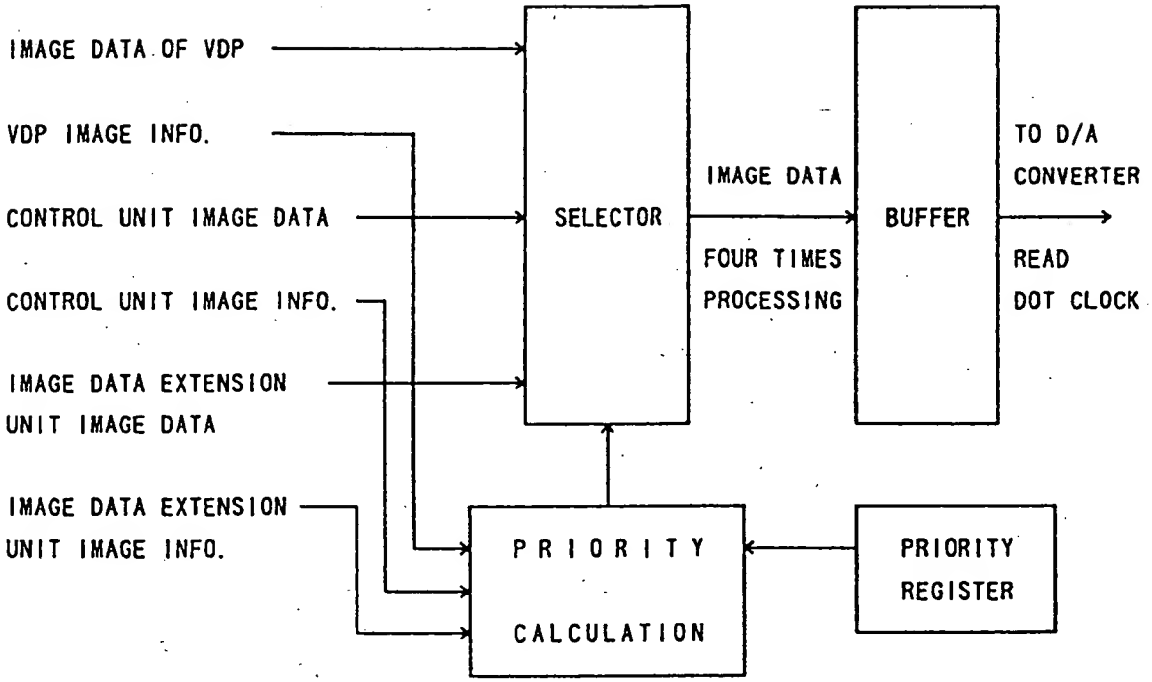
IMAGE DATA OF VDP
VDP IMAGE INFO.
CONTROL UNIT IMAGE DATA
CONTROL UNIT IMAGE INFO.
IMAGE DATA EXTENSION UNIT IMAGE DATA
IMAGE DATA EXTENSION UNIT IMAGE INFO.
SELECTOR
IMAGE DATA
FOUR TIMES PROCESSING
BUFFER
TO D/A CONVERTER
READ DOT CLOCK
PRIORITY CALCULATION
PRIORITY REGISTER

FIG. 8

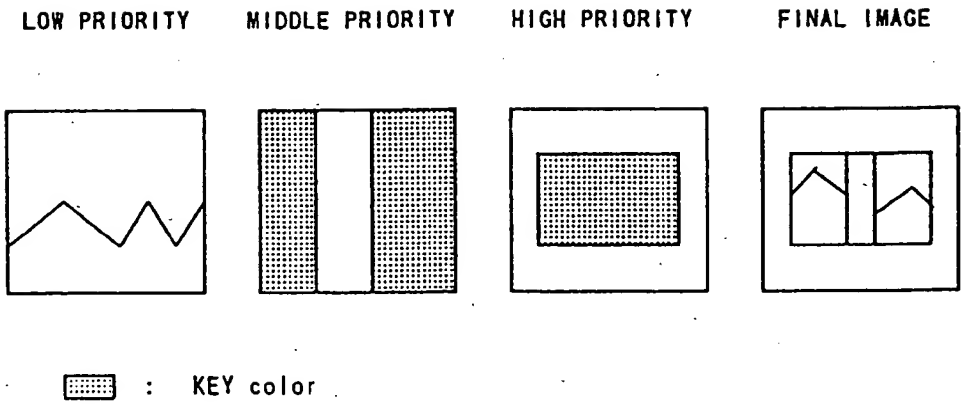
LOW PRIORITY
MIDDLE PRIORITY
HIGH PRIORITY
FINAL IMAGE
: KEY color

FIG. 9A

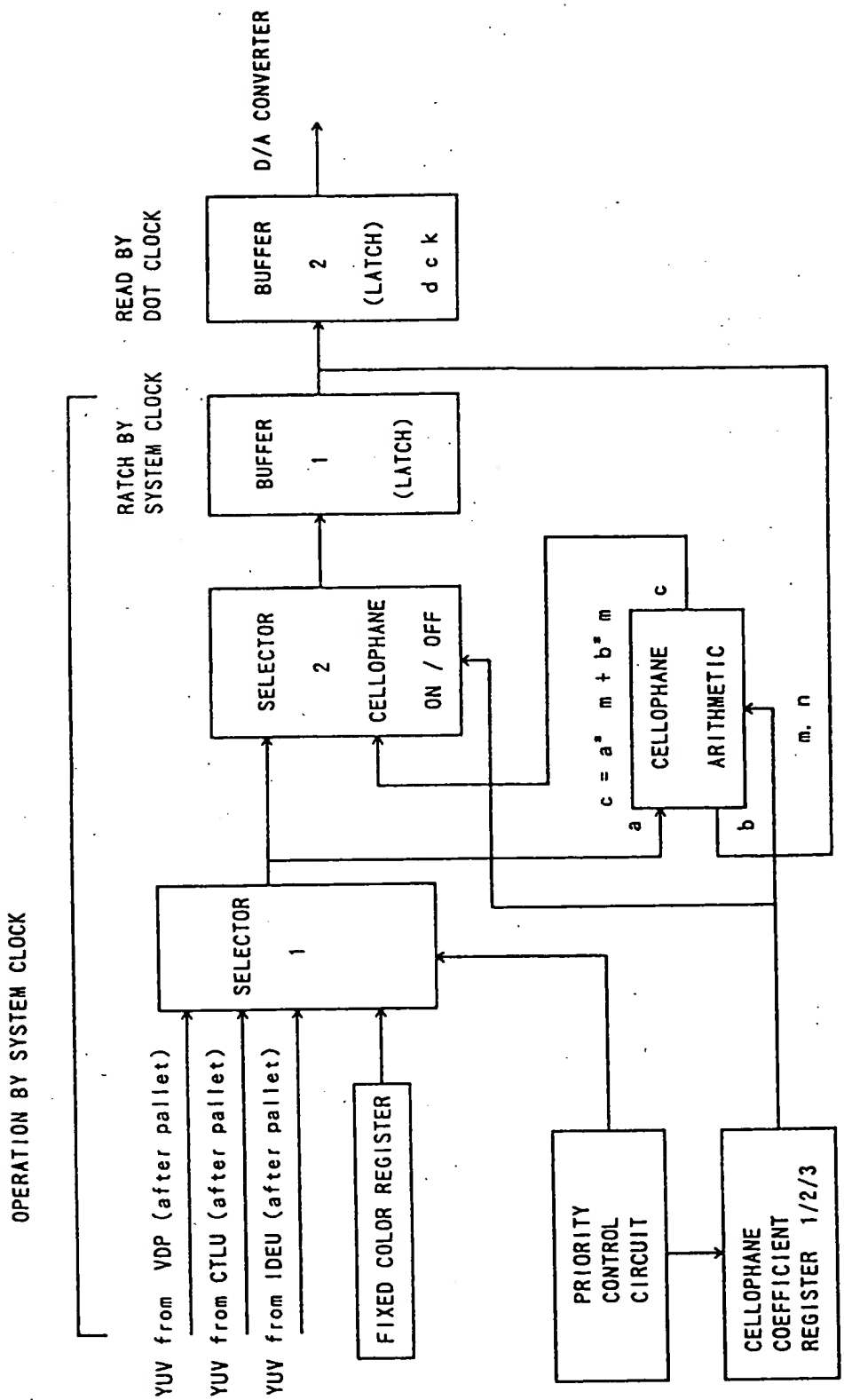
OPERATION BY SYSTEM CLOCK
YUV from VDP (after pallet)
YUV from CTLU (after pallet)
YUV from IDEU (after pallet)
SELECTOR 1
FIXED COLOR REGISTER
PRIORITY CONTROL CIRCUIT
CELLOPHANE COEFFICIENT REGISTER 1/2/3
SELECTOR 2 CELLOPHANE ON / OFF
c = a* m + b* m
a
b
c
CELLOPHANE ARITHMETIC
m, n
RATCH BY SYSTEM CLOCK
BUFFER 1 (LATCH)
READ BY DOT CLOCK
BUFFER 2 (LATCH) d c k
D/A CONVERTER

FIG. 9B

PICTURE			
VDP	SPRITE	COLOR PALLET DATA	PALLET No. 0(ALL PALLET BANK)
	BG	COLOR PALLET DATA	PALLET No. 0(ALL PALLET BANK)
CONTROL UNIT (RL PICTURE)	16M COLOR MODE	YUV DATA	Y DATA = 00h
	64K COLOR MODE	YUV DATA	Y DATA = 00h
	4 COLOR MODE	COLOR PALLET DATA	COLOR PALLET DATA 0
	16 COLOR MODE	COLOR PALLET DATA	COLOR PALLET DATA 0
	256 COLOR MODE	COLOR PALLET DATA	COLOR PALLET DATA 0
	INVALID	INVALID	ANY DATA
IMAGE-DATA EXTENSION UNIT	IDCT	YUV DATA	SET COLOR OF REGISTER
	RL 16 COLOR MODE	COLOR PALLET DATA	PALLET No. 0
	RL 32 COLOR MODE	COLOR PALLET DATA	PALLET No. 0
	RL 64 COLOR MODE	COLOR PALLET DATA	PALLET No. 0
	RL128 COLOR MODE	COLOR PALLET DATA	PALLET No. 0
	INVALID	INVALID	ANY DATA

FIG. 11

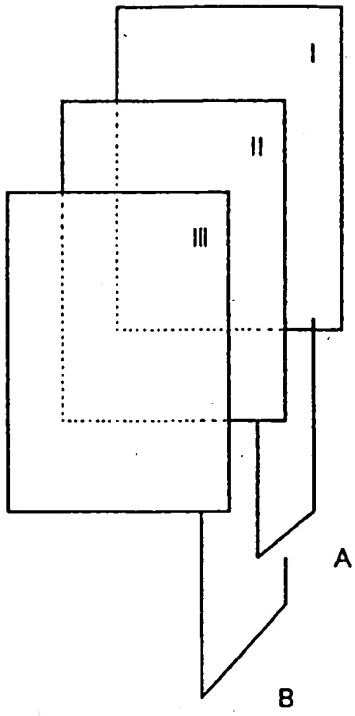

FIG. 12

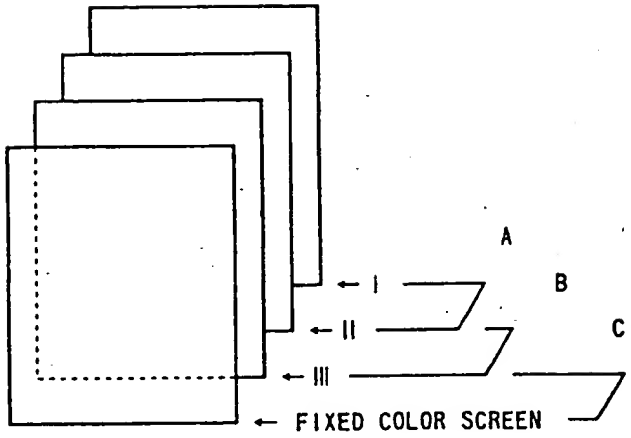
A
B
C
← I
← II
← III
← FIXED COLOR SCREEN

FIG. 13

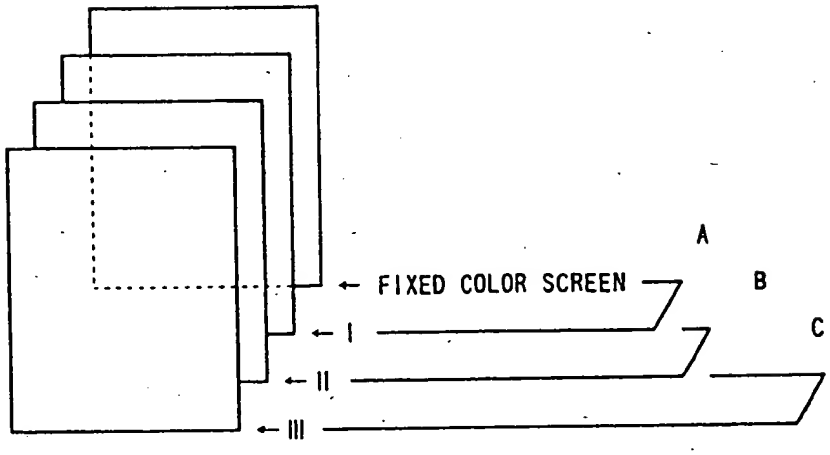
A
B
C
← FIXED COLOR SCREEN
← I
← II
← III

FIG. 14

(ADDRESS REGISTER)

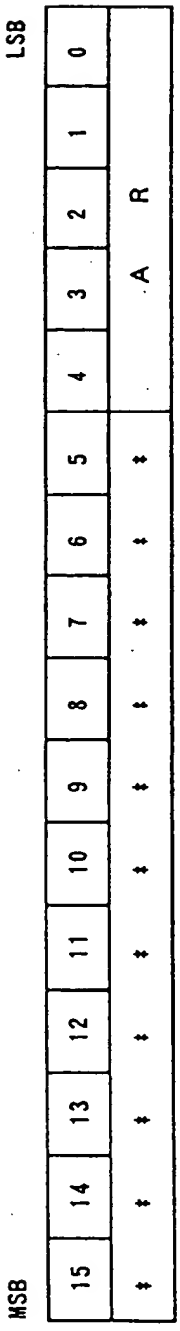

FIG. 15

(STATUS REGISTER)

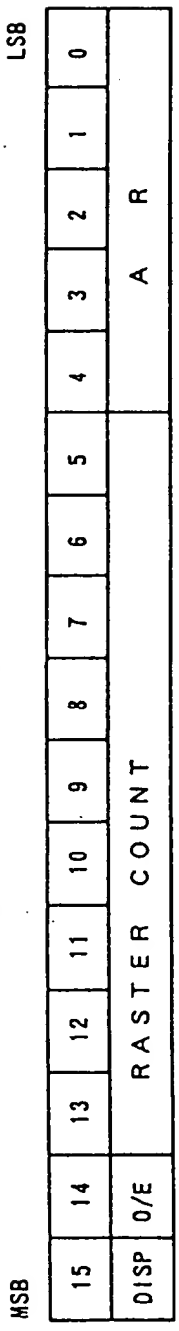

FIG. 16

(CONTROL REGISTER)

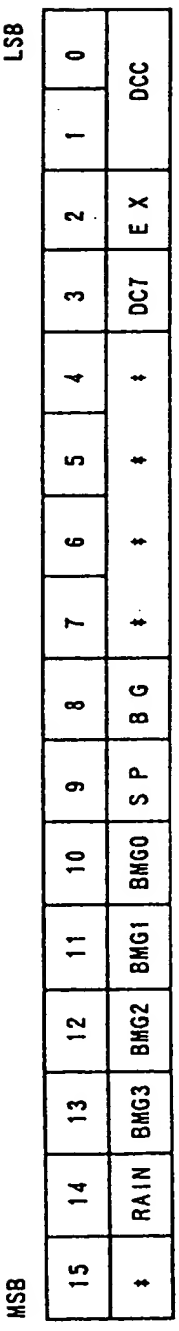

FIG. 18

(COLOR PALLET ADDRESS REGISTER)

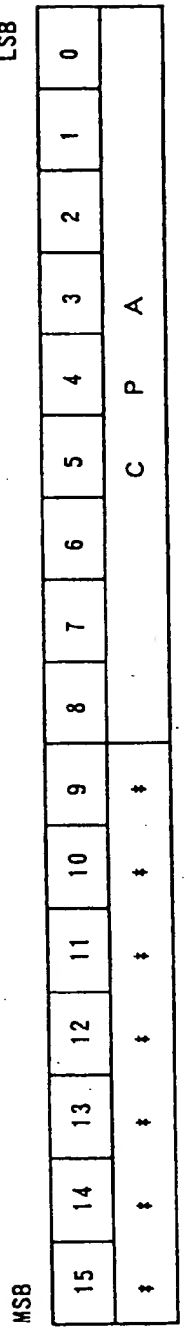

FIG. 19

(COLOR PALLET DATA WRITE REGISTER)

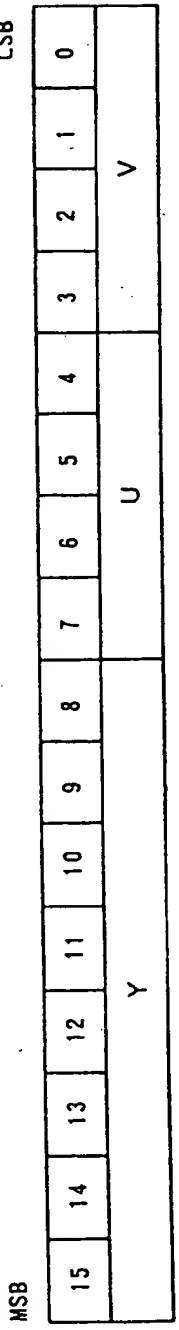

FIG. 20

(COLOR PALLET ADDRESS OFFSET REGISTER 1)

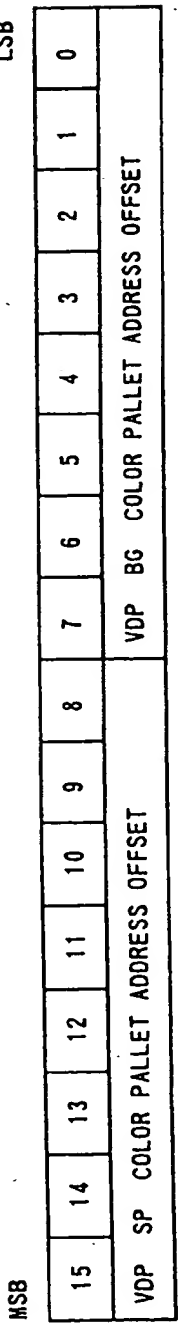

FIG. 21

(COLOR PALLET ADDRESS OFFSET REGISTER 2)

MSB															LSB
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CTRU BMG 1 COLOR PALLET ADDRESS OFFSET								CTRU BMG 0 COLOR PALLET ADDRESS OFFSET							

FIG. 22

(COLOR PALLET ADDRESS OFFSET REGISTER 3)

MSB															LSB
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CTRU BMG 3 COLOR PALLET ADDRESS OFFSET								CTRU BMG 2 COLOR PALLET ADDRESS OFFSET							

FIG. 23

(COLOR PALLET ADDRESS OFFSET REGISTER 4)

MSB															LSB
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
*	*	*	*	*	*	*	*	IMAGE DATA EXTENSION UNIT COLOR PALLET ADDRESS OFFSET							

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FIG. 24

(PRIORITY REGISTER 1)

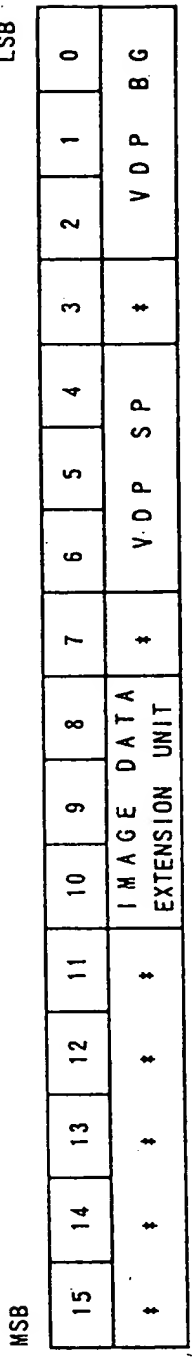

FIG. 25

(PRIORITY REGISTER 2)

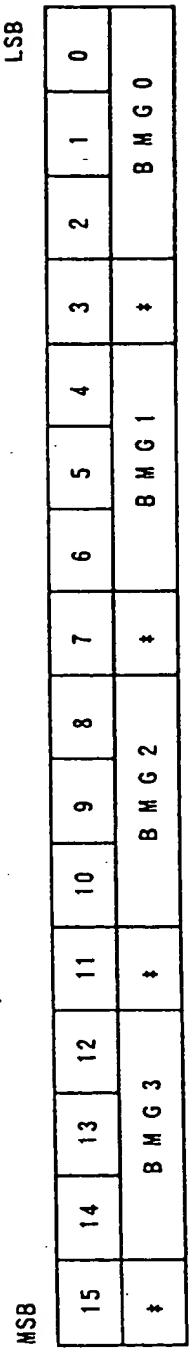

FIG. 26

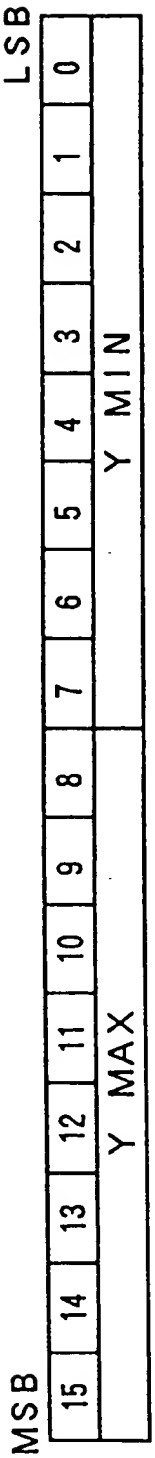

FIG. 27

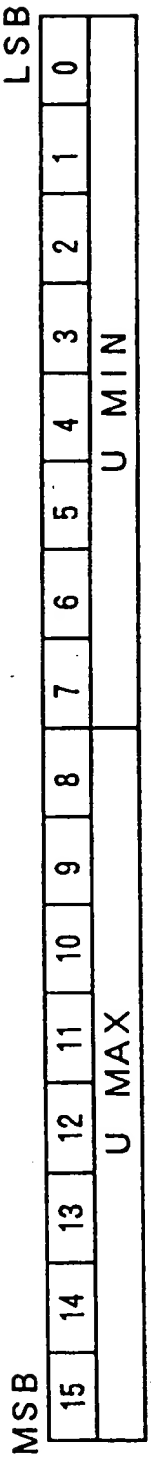

FIG. 28

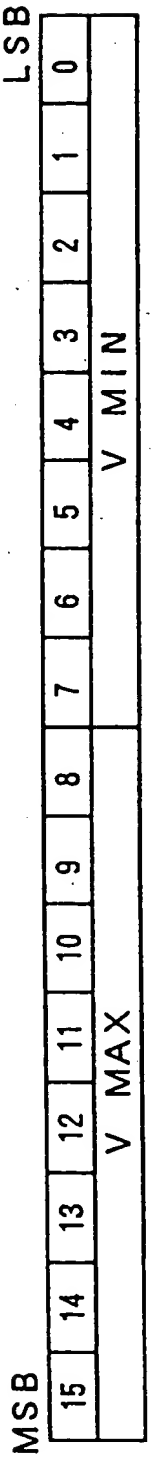

FIG. 29

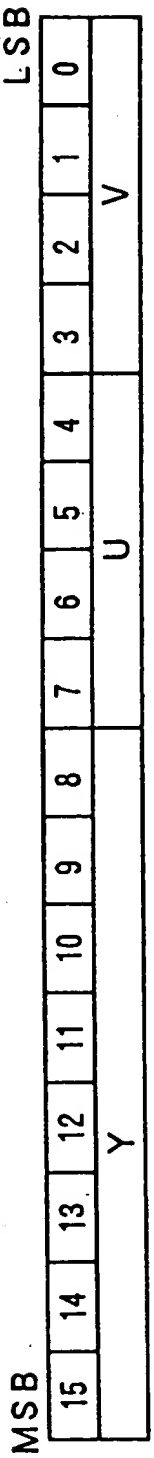

FIG. 30

MSB LSB

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F/B	E/D	IDU		CTRL BMG3		CTRL BMG3		CTRL BMG1		CTRU BMG0		VDP SP		VDP BG	

FIG. 31

VDP BG bit		CONTENT
1	0	
0	0	CELLOPHANE OFF
0	1	CELLOPHANE ON CELLOPHANE REGISTER 1A/B
1	0	CELLOPHANE ON CELLOPHANE REGISTER 2A/B
1	1	CELLOPHANE ON CELLOPHANE REGISTER 3A/B

FIG. 32

VDP SP bit		CONTENT
3	2	
0	0	CELLOPHANE OFF
0	1	CELLOPHANE ON CELLOPHANE REGISTER 1A/B
1	0	CELLOPHANE ON CELLOPHANE REGISTER 2A/B
1	1	CELLOPHANE ON CELLOPHANE REGISTER 3A/B

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FIG. 33

CTRLU BMG0 bit		CONTENT
5	4	
0	0	CELLOPHANE OFF
0	1	CELLOPHANE ON CELLOPHANE REGISTER 1A/B
1	0	CELLOPHANE ON CELLOPHANE REGISTER 2A/B
1	1	CELLOPHANE ON CELLOPHANE REGISTER 3A/B

FIG. 34

CTRLU BMG1 bit		CONTENT
7	6	
0	0	CELLOPHANE OFF
0	1	CELLOPHANE ON CELLOPHANE REGISTER 1A/B
1	0	CELLOPHANE ON CELLOPHANE REGISTER 2A/B
1	1	CELLOPHANE ON CELLOPHANE REGISTER 3A/B

FIG. 35

CTRLU BMG2 bit		CONTENT
9	8	
0	0	CELLOPHANE OFF
0	1	CELLOPHANE ON CELLOPHANE REGISTER 1A/B
1	0	CELLOPHANE ON CELLOPHANE REGISTER 2A/B
1	1	CELLOPHANE ON CELLOPHANE REGISTER 3A/B

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FIG. 36

CTRLU BMG3 bit		CONTENT
11	10	
0	0	CELLOPHANE OFF
0	1	CELLOPHANE ON CELLOPHANE REGISTER 1A/B
1	0	CELLOPHANE ON CELLOPHANE REGISTER 2A/B
1	1	CELLOPHANE ON CELLOPHANE REGISTER 3A/B

FIG. 37

IDU bit		CONTENT
13	12	
0	0	CELLOPHANE OFF
0	1	CELLOPHANE ON CELLOPHANE REGISTER 1A/B
1	0	CELLOPHANE ON CELLOPHANE REGISTER 2A/B
1	1	CELLOPHANE ON CELLOPHANE REGISTER 3A/B

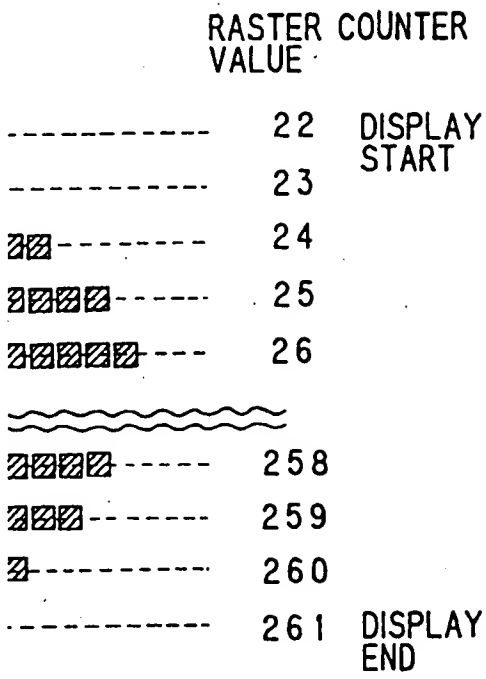

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FIG. 38

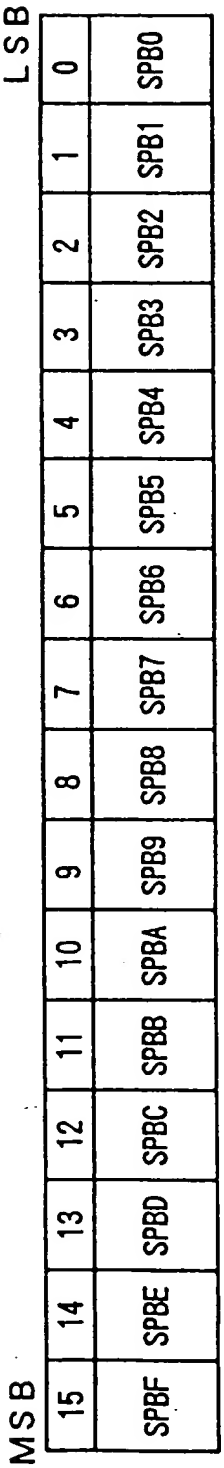

MSB
LSB
15
14
13
12
11
10
9
8
7
6
5
4
3
2
1
0
SPBF
SPBE
SPBD
SPBC
SPBB
SPBA
SPB9
SPB8
SPB7
SPB6
SPB5
SPB4
SPB3
SPB2
SPB1
SPB0

FIG. 39

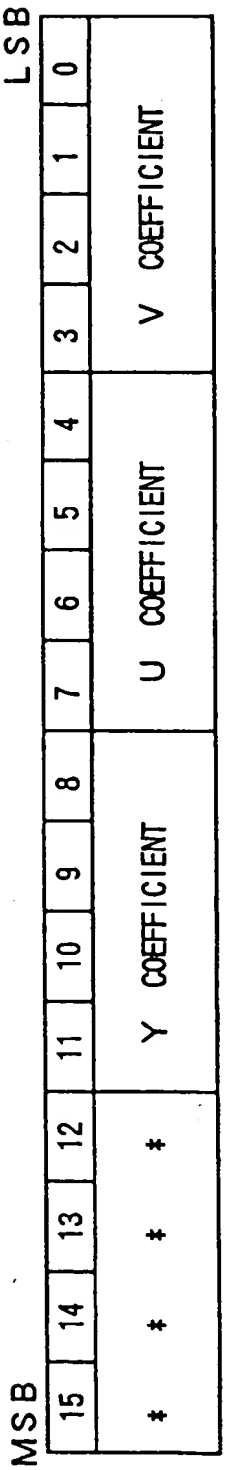

MSB
LSB
15
14
13
12
11
10
9
8
7
6
5
4
3
2
1
0
* * * *
Y COEFFICIENT
U COEFFICIENT
V COEFFICIENT

FIG. 40

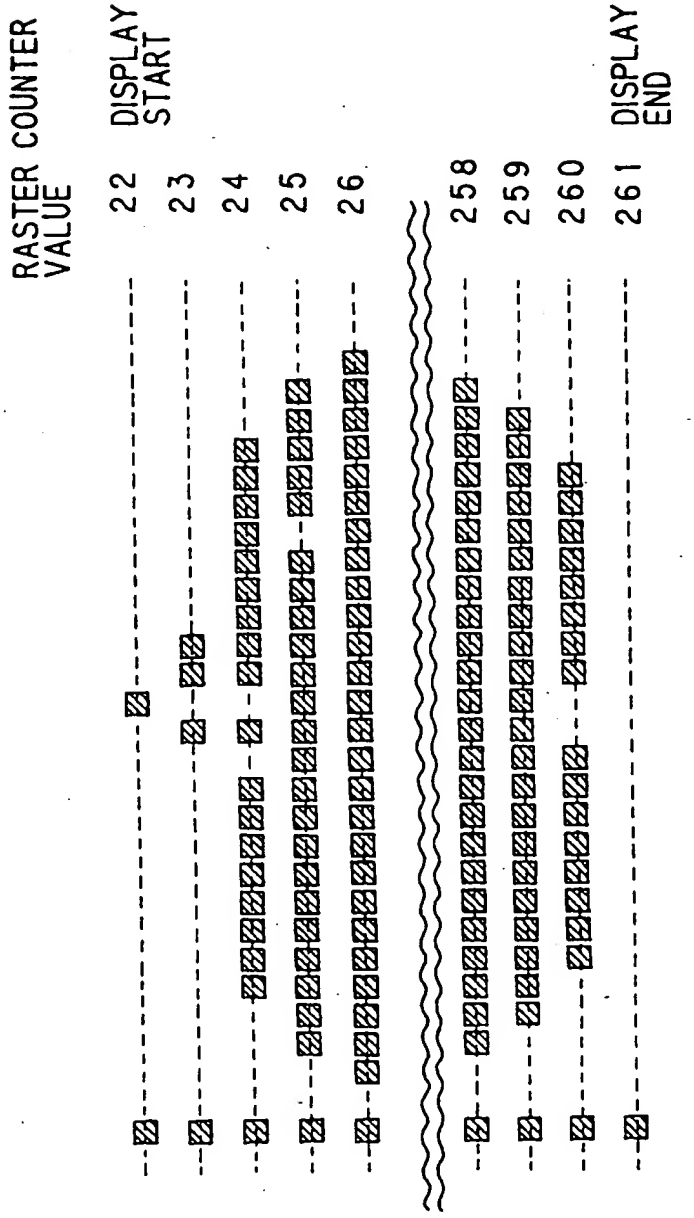

RASTER COUNTER VALUE
22
DISPLAY START
23
24
25
26
258
259
260
261
DISPLAY END

FIG. 41

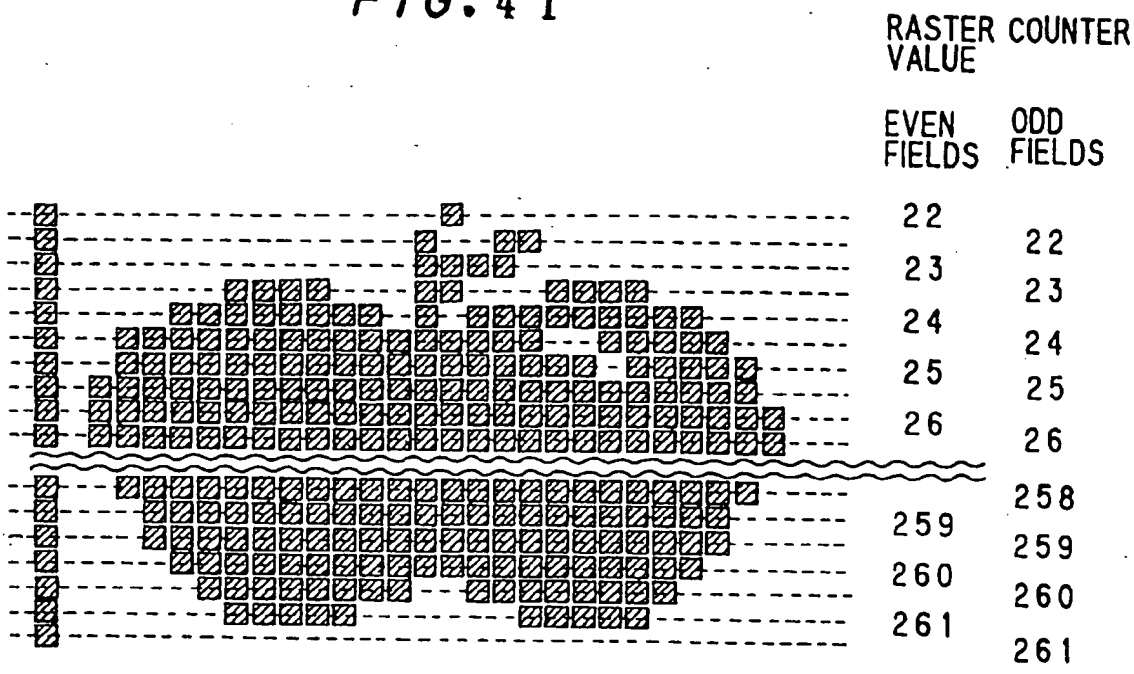
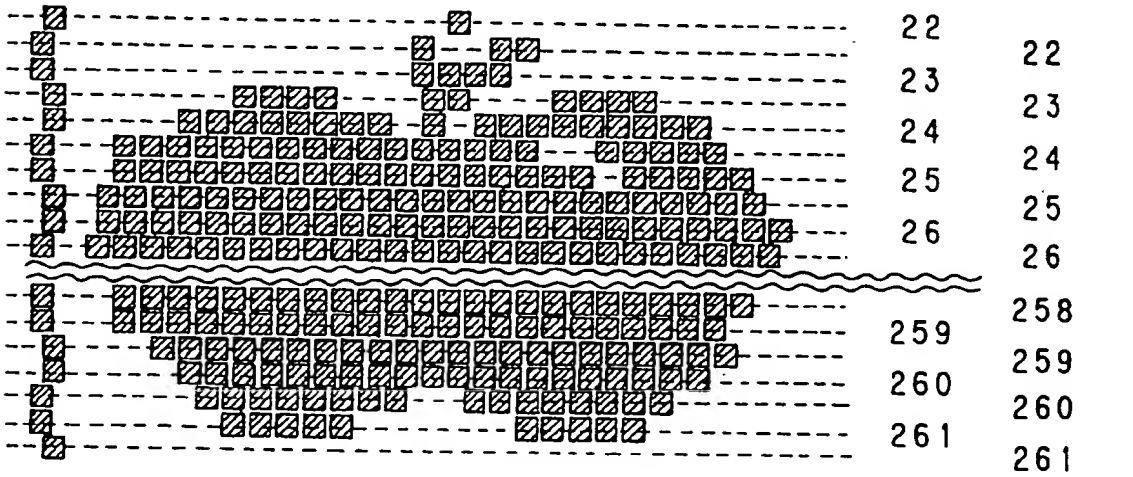

RASTER COUNTER VALUE
EVEN FIELDS
ODD FIELDS
22
22
23
23
24
24
25
25
26
26
258
259
259
260
260
261
261

FIG. 42


22
22
23
23
24
24
25
25
26
26
258
259
259
260
260
261
261